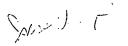What is claimed is:

1. 1. A delay measurement circuit comprising:

2 first and second channels for receiving first and second

3 signals, each of said signals having a leading edge and a

4 trailing edge;

5 a leading edge circuit coupled to said first and said

6 second channels for signaling the temporal relationship of

7 the leading edges of said first and said second signals;

8 a trailing edge circuit coupled to said first and said

9 second channels for signaling the temporal relationship of

10 the trailing edges of said first and said second signals;

11 a memory coupled to said leading edge circuit for storing

12 data of said leading edges;

13 timing means activated by said leading edge circuit for

14 measuring a delay between leading edges of said first and said

15 second signals; and

16 gating means coupled to said memory in said trailing edge

17 circuit for reading out data of said timing means when data

18 stored in said memory conforms to said temporal relationship

19 signal by said trailing edge circuit.

1 2. A delay measurement circuit providing a differential

2 delay measurement free of noise induced bias errors comprising:

3 means for measuring the differential delay between the

4 leading edges of two signals;

5 means for comparing a temporal relationship of the trailing

6 edges of said two signals with a temporal relationsip of said

7 leading edges; and

8 means for discarding a measure of said measuring means when

9 said temporal relationship of said trailing edges fails to

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10   conform with said temporal relationship of said leading edges.

1   (U)   3. A delay measurement circuit according to Claim 2

2   further comprising a memory coupled to said delay measurement

3   means for recording said temporal relationship between said

4   leading edges to permit a subsequent comparison of said temporal

5   relationship of said leading edges with said temporal relationship

6   of said trailing edges.

DMW:df

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